ABSTRACT

COMPUTER SYSTEM

A computer system is arranged to provide protection against faults. The computer system comprises a plurality of processing sets (14, 16), each having at least one processor (52) and a bridge (12) coupled to each of the processing sets (14, 16) and operable to monitor a step locked operation of said processing sets (14, 16). Each of the processors (52) has a processor identification register (64) which is read/writeable and is operable to store in the register data representative of a processor identification. The processors (14, 16) are arranged, consequent upon a masking condition, to load a common predefined data value into the processor identification register, which predefined common data value has an effect of masking the processor identification. The erroneous detection by the bridge (12) of a fault condition resulting from functionally the same processors having a different processor identification is thereby avoided, or at least the likelihood of a false detection reduced. The masking condition may be, for example, a boot or re-boot of a processing set, or a forced re-configuration or initialization of the processing system instigated by an operating system.

Figure 6 for Abstract